

CLAIMS

What is claimed is:

- 1 1. A process comprising:
2 in a substrate, forming a first isolation structure spaced-apart from a
3 second isolation structure;
4 forming an emitter stack between the first and second isolation
5 structures;
6 in the substrate, forming a self-aligned recess between the emitter
7 stack and the first isolation structure; and
8 forming a bipolar junction transistor between the first and second
9 isolation structures.
- 1 2. The process according to claim 1, further including:
2 implanting a self-aligned collector tap in the self-aligned recess.
- 1 3. The process according to claim 1, wherein forming a self-aligned
2 recess further includes:
3 patterning a mask that exposes a portion of the first isolation
4 structure, a portion of the emitter stack, and a portion of the substrate located
5 between the first isolation structure and the emitter stack; and
6 etching the self-aligned recess with an etch recipe that is more
7 selective to the first isolation structure and the emitter stack than to the
8 substrate.
- 1 4. The process according to claim 1, wherein forming a self-aligned
2 recess further includes:
3 patterning a mask that exposes a portion of the first isolation
4 structure, a portion of the emitter stack, and a portion of the substrate located
5 between the first isolation structure and the emitter stack; and

6 anisotropically etching the self-aligned recess with an etch recipe that
7 is more selective to the first isolation structure and the emitter stack than to
8 the substrate.

1 5. The process according to claim 1, wherein implanting a self-aligned
2 collector tap in the self-aligned recess includes:

3 patterning a mask that exposes at least a portion of the first isolation
4 structure and the emitter stack; and
5 implanting a dopant into the substrate that is exposed by the self-
6 aligned recess.

1 6. The process according to claim 1, wherein implanting a self-aligned
2 collector tap in the self-aligned recess includes:

3 patterning a mask that exposes at least a portion of the first isolation
4 structure and the emitter stack; and
5 implanting a dopant into the substrate that is exposed by the recess,
6 wherein implanting results in a P-- collector tap, a P- collector tap, a P
7 collector tap, a P+ collector tap, a P++ collector tap, an N-- collector tap, an
8 N- collector tap, an N collector tap, an N+ collector tap, and an N++
9 collector tap.

1 7. The process according to claim 1, wherein forming the bipolar
2 junction transistor between the first and second isolation structures includes:

3 in the substrate, forming an epitaxial layer;
4 forming a polysilicon film above the epitaxial layer; and
5 patterning the polysilicon film into emitter polysilicon.

1 8. The process according to claim 1, wherein forming the bipolar
2 junction transistor between the first and second isolation structures includes:

3 in the substrate, forming an epitaxial layer;
4 forming a polysilicon film above the epitaxial layer;

5 patterning the polysilicon film into emitter polysilicon; and
6 forming a spacer on the emitter stack.

1 9. The process according to claim 1, wherein forming the bipolar
2 junction transistor between the first and second isolation structures includes:
3 in the substrate, implanting a collector structure;
4 in the substrate, forming an epitaxial layer;
5 forming a polysilicon film over the epitaxial layer; and
6 patterning the polysilicon film into emitter polysilicon, wherein the
7 emitter polysilicon is disposed above the collector structure.

1 10. The process according to claim 1, wherein forming an emitter stack
2 includes:
3 in the substrate, forming an epitaxial layer;
4 forming a polysilicon film above the epitaxial layer;
5 patterning the polysilicon film into emitter polysilicon, wherein
6 patterning the polysilicon film into emitter polysilicon further includes:
7 patterning a hard mask above the polysilicon film.

1 11. The process according to claim 1, wherein forming an emitter stack
2 includes:
3 in the substrate, forming an epitaxial layer;
4 forming a dielectric layer above the epitaxial layer;
5 forming an emitter cut in the dielectric layer;
6 forming a polysilicon film above the epitaxial layer; and
7 patterning the polysilicon film into emitter polysilicon.

1 12. The process according to claim 1, further including:
2 in the substrate, forming a buried layer.

1 13. A bipolar junction transistor comprising:
2 in a substrate, a first isolation structure spaced apart from a second
3 isolation structure;
4 an emitter stack disposed above the substrate and between the first
5 isolation structure and the second isolation structure;
6 a recess disposed adjacent and between the emitter stack and the first
7 isolation structure, wherein the recess exposes a collector tap.

1 14. The bipolar junction transistor according to claim 13, further
2 including:
3 a spacer disposed on the emitter stack, wherein the spacer extends on
4 one side thereof into the recess between the emitter stack and the first
5 isolation structure.

1 15. The bipolar junction transistor according to claim 13, further
2 including:
3 a spacer disposed on the emitter stack, wherein the spacer extends on
4 one side thereof into the recess between the emitter stack and the first
5 isolation structure, and wherein the spacer is selected from an oxide, a
6 nitride, an oxide first layer and a nitride second layer, a nitride first layer and
7 an oxide second layer, an oxide first layer and an oxide second layer, and a
8 nitride first layer and a nitride second layer.

1 16. The bipolar junction transistor according to claim 13, further
2 including:
3 a spacer disposed on the emitter stack, wherein the spacer extends on
4 one side thereof into the recess between the emitter stack and the first
5 isolation structure, and wherein the spacer is further disposed on the first
6 isolation structure and extends into the recess.

1 17. The bipolar junction transistor according to claim 13, further
2 including:
3 a buried layer disposed in the substrate between the first isolation
4 structure and the second isolation structure.

1 18. The bipolar junction transistor according to claim 13, further
2 including:
3 in the substrate, an epitaxial base layer disposed below the emitter
4 stack;
5 a collector structure disposed in the substrate below the emitter stack;
6 and
7 an intrinsic base structure disposed between the emitter stack and the
8 collector structure.

1 19. The bipolar junction transistor according to claim 13, further
2 including:
3 in the substrate, an epitaxial base layer disposed below the emitter
4 stack;
5 a collector structure disposed in the substrate below the emitter stack;
6 a dielectric layer disposed above the substrate and below the emitter
7 stack, wherein the dielectric layer includes an emitter cut disposed above the
8 collector structure; and
9 an intrinsic base structure disposed between the emitter cut and the
10 collector structure.

1 20. The bipolar junction transistor according to claim 13, further
2 including:
3 in the substrate, a collector tap disposed in the recess, wherein the
4 collector tap is selected from a P-- collector tap, a P- collector tap, a P
5 collector tap, a P+ collector tap, a P++ collector tap, an N-- collector tap, an

6 N- collector tap, an N collector tap, an N+ collector tap, and an N++
7 collector tap.

1 21. The bipolar junction transistor according to claim 13, wherein the
2 substrate includes a bipolar-complementary metal oxide semiconductor
3 (BiCMOS) structure.

1 22. The bipolar junction transistor according to claim 13, wherein the
2 BJT is selected from a monojunction BJT device and a heterojunction BJT device.

1 23. A bipolar junction transistor (BJT) layout comprising:
2 an epitaxial base layer perimeter;
3 an emitter stack perimeter disposed above the base layer perimeter;
4 and
5 a collector tap perimeter, wherein the emitter stack perimeter and the
6 collector tap perimeter share a co-linear first boundary.

1 24. The BJT layout according to claim 23, wherein the emitter stack
2 perimeter and the epitaxial base layer perimeter intersect.

1 25. The BJT layout according to claim 23, wherein the collector tap
2 perimeter shares a co-linear second boundary and a co-linear third boundary with
3 the epitaxial base layer perimeter.

1 26. The BJT layout according to claim 23, further including:
2 a base tap perimeter, wherein the base tap perimeter is enclosed by
3 the epitaxial base layer perimeter.